What is claimed is:

1. A failure analysis system of a logic LSI having software incorporated therein comprising:

a function to record the terminal signal information of said logic LSI in synchronization with a clock;

a function to reproduce said recorded terminal signal information in synchronization with the clock; and

a function to compare said reproduced terminal signal information with the terminal signal information of a normal logic LSI.

2. A failure analysis system of a logic LSI having software incorporated therein comprising:

a function to record the terminal signal information of the logic LSI as a target of analysis in synchronization with a clock;

a function to record the terminal signal information of a normal logic LSI in synchronization with a clock; and

a function to compare said recorded terminal signal information of the logic LSI as the target of analysis with said recorded terminal signal information of the normal logic LSI.

3. A failure analysis system of a logic LSI having software incorporated therein comprising:

a function to record the terminal signal information of the logic LSI as a target of analysis in synchronization with

a clock;

a function to reproduce said recorded terminal signal information in synchronization with a clock; and

a function to compare said reproduced terminal signal information of the logic LSI as the target of analysis with the terminal signal information of an emulator of a logic LSI.

4. A failure analysis system of a logic LSI having software incorporated therein comprising:

a function to record the terminal signal information of the logic LSI as a target of analysis in synchronization with a clock; and

a function to compare said recorded terminal signal information of the logic LSI as the target of analysis with the terminal signal information of the emulator of the logic LSI.

5. A failure analysis system of a logic LSI according to claim 1, wherein said terminal signal information includes a trace data map of the condition change in the register data and the RAM data for a specific time of period.

6. A failure analysis system of a logic LSI according to claim 1, wherein said failure analysis system further has a function to generate a trace difference map of the trace data map of the logic LSI as the analysis target and the trace data map of the normal logic LSI.

7. A failure analysis system of a logic LSI according

to claim 1, wherein said failure analysis system further has a function to generate a plurality of said trace difference maps by generating a plurality of defects and to obtain the average and the data spread of the difference by a statistical work.

8. A failure analysis system of a logic LSI according to claim 1, wherein said failure analysis system further has a function to save the conditions of the RAM and the register before generation of the defect and to resume the conditions of the RAM and the register from the conditions before generation of the defect.

9. A failure analysis system of a logic LSI according to claim 1, wherein said failure analysis system further has a function to record the command trace data of a CPU in synchronization with said terminal signal information.

10. A failure analysis system of a logic LSI according to claim 1, wherein said failure analysis system further has a function to vary a reproduction speed of said terminal signal.

11. A failure analysis system of a logic LSI according to claim 1, wherein said failure analysis system further has a function to connect comparative signals of a plurality of logic LSIs to multiinput OR terminals and to analyze a plurality of logic LSIs at the same time.

12. A failure analysis system of a logic LSI according to claim 1, wherein said terminal signal information also

includes the analog signal information.

13. A failure analysis system of a logic LSI according to claim 12, wherein said failure analysis system further has a function to obtain in advance analog/digital difference properties of the logic LSI as the analysis target and the normal logic LSI, or digital/analog difference properties thereof and to correct an analog conversion property.

14. A failure analysis system of a logic LSI according to claim 12, wherein said logic LSI has an on-chip debugger mounted thereon.

15. A failure analysis system of a logic LSI according to claim 1, wherein said failure analysis system further has layered software.

16. A failure analysis system of a logic LSI according to claim 1, wherein the analysis target is a system having a logic LSI mounted thereon.

17. A failure analysis method of a logic LSI having software incorporated therein comprising:

means to record the terminal signal information of said logic LSI in synchronization with a clock;

means to reproduce said recorded terminal signal information in synchronization with the clock; and

means to compare said reproduced terminal signal information with the terminal signal information of a normal logic LSI.

18. A failure analysis method of a logic LSI having software incorporated therein comprising:

means to record the terminal signal information of the logic LSI as a target of analysis in synchronization with a clock;

means to record the terminal signal information of a normal logic LSI in synchronization with a clock; and

means to compare said recorded terminal signal information of the logic LSI as the target of analysis with said recorded terminal signal information of the normal logic LSI.

19. A failure analysis method of a logic LSI having software incorporated therein comprising:

means to record the terminal signal information of the logic LSI as a target of analysis in synchronization with a clock;

means to reproduce said recorded terminal signal information in synchronization with a clock; and

means to compare said reproduced terminal signal information of the logic LSI as the target of analysis with the terminal signal information of an emulator of a logic LSI.

20. A failure analysis method of a logic LSI having software incorporated therein comprising:

means to record the terminal signal information of the logic LSI as a target of analysis in synchronization with a

clock; and

means to compare said recorded terminal signal information of the logic LSI as the target of analysis with the terminal signal information of the emulator of the logic LSI.

21. A failure analysis method of a logic LSI according to claim 17, wherein said terminal signal information includes a trace data map of the condition change in the register data and the RAM data for a specific time of period.

22. A failure analysis method of a logic LSI according to claim 17, wherein said failure analysis method further has means to generate a trace difference map of the trace data map of the logic LSI as the analysis target and the trace data map of the normal logic LSI.

23. A failure analysis method of a logic LSI according to claim 17, wherein said failure analysis method further has means to generate a plurality of said trace difference maps by generating a plurality of defects and to obtain the average and the data spread of the difference by a statistical work.

24. A failure analysis method of a logic LSI according to claim 17, wherein said failure analysis method further has means to save the conditions of the RAM and the register before generation of the defect and to resume the conditions of the RAM and the register from the conditions before generation of the defect.

25. A failure analysis method of a logic LSI according to claim 17, wherein said failure analysis method further has means to record the command trace data of a CPU in synchronization with said terminal signal information.

26. A failure analysis method of a logic LSI according to claim 17, wherein said failure analysis method further has means to vary a reproduction speed of said terminal signal.

27. A failure analysis method of a logic LSI according to claim 17, wherein said failure analysis method further has means to connect comparative signals of a plurality of logic LSIs to multiinput OR terminals and to analyze a plurality of logic LSIs at the same time.

28. A failure analysis method of a logic LSI according to claim 17, wherein said terminal signal information also includes the analog signal information.

29. A failure analysis method of a logic LSI according to claim 28, wherein said failure analysis method further has means to obtain in advance analog/digital difference properties of the logic LSI as the analysis target and the normal logic LSI, or digital/analog difference properties thereof and to correct an analog conversion property.

30. A failure analysis method of a logic LSI according to claim 28, wherein said logic LSI has an on-chip debugger mounted thereon.

31. A failure analysis method of a logic LSI according

to claim 17, wherein the analysis target is a system having a logic LSI mounted thereon.